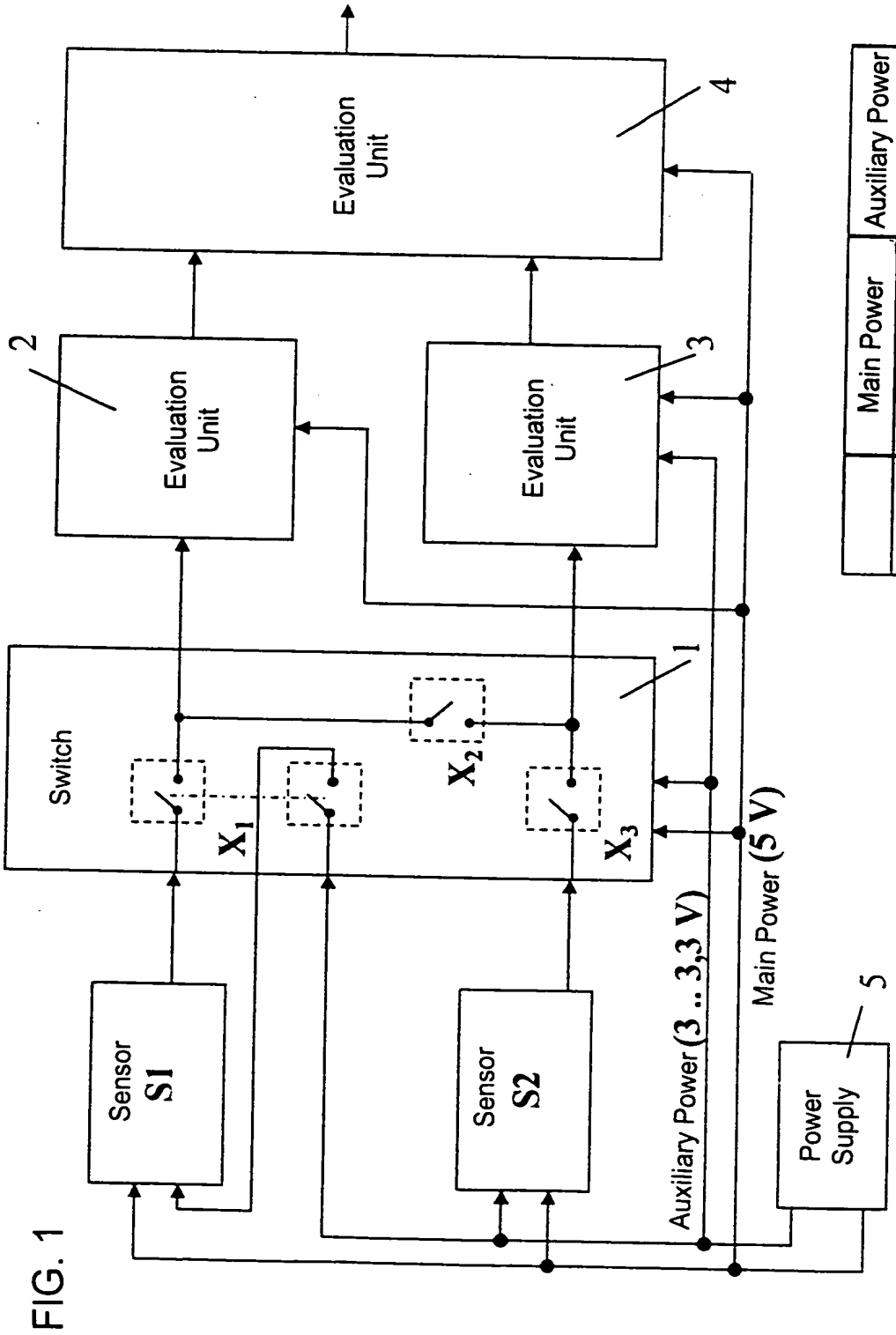

FIG. 1

	Main Power			Auxiliary Power		
	X_1	X_2	X_3	X_1	X_2	X_3
S1 + S2	1	0	1	0	0	1
S1	1	1	0	1	1	0
S2	0	1	1	0	0	1

FIG. 1A

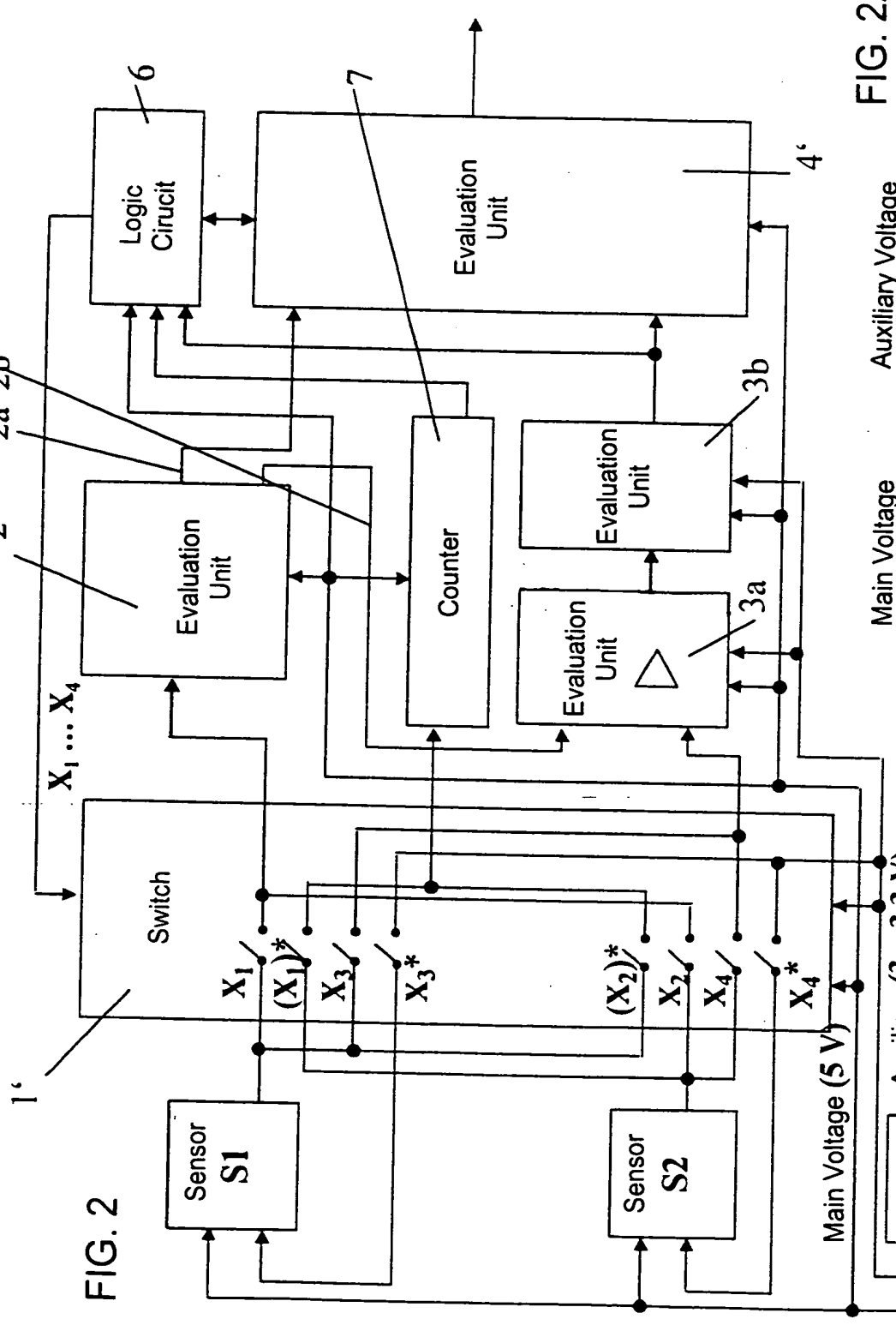

FIG. 2

	Main Voltage				Auxiliary Voltage			
	X_1	X_2	X_3	X_4	X_1	X_2	X_3	X_4
S_1	1	-/(1)*	0	-	0	-/(0)*	1	-
S_2	-/(1)*	1	-	0	-(0)*	0	-	1
S_1 (S_2)	1	0/(1)*	0	0	0	0/(0)*	1	0
S_2 (S_1)	0/(1)*	1	0	0	0/(0)*	0	0	1

FIG. 2A

FIG. 3

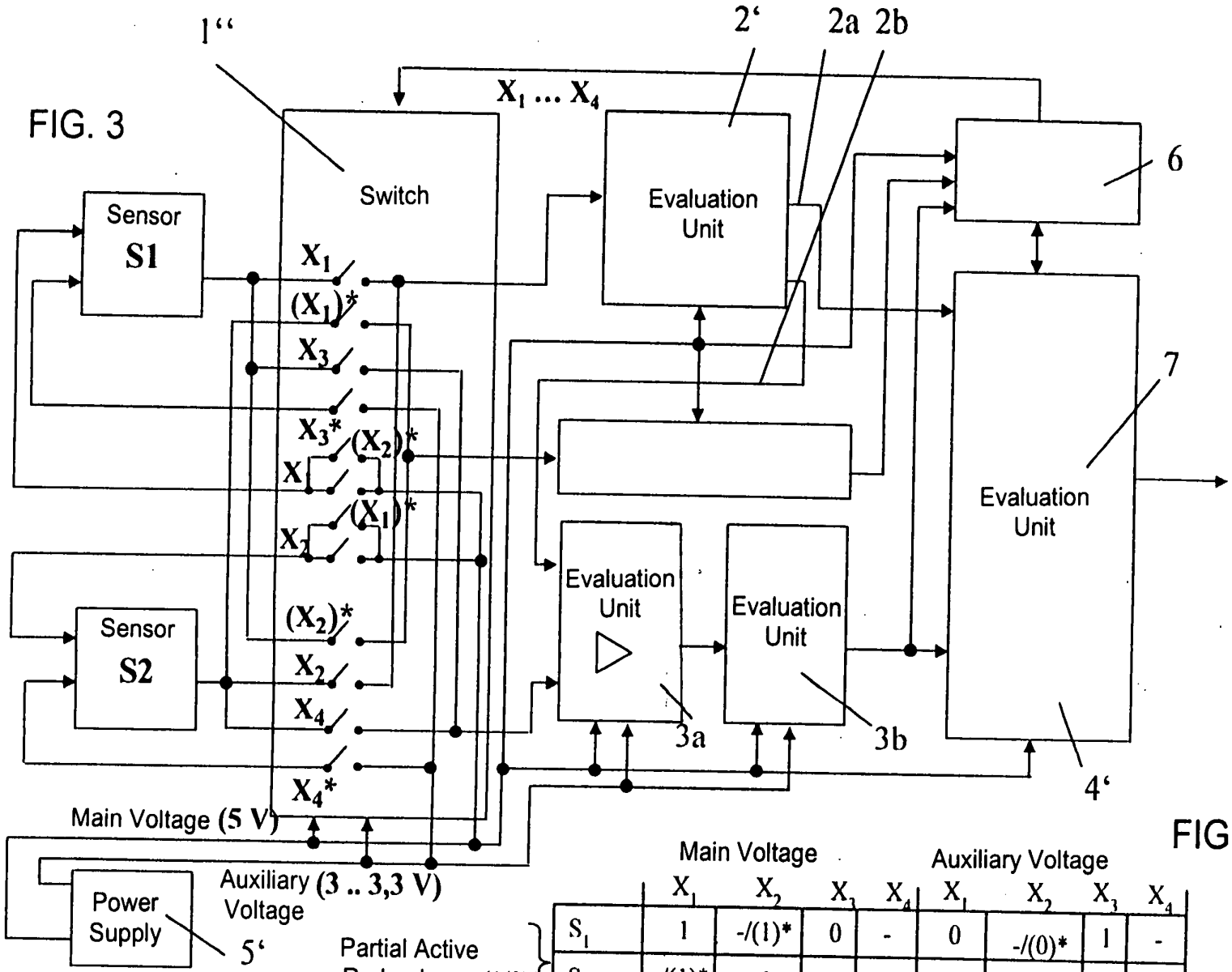

FIG. 3A

	Main Voltage				Auxiliary Voltage			
	X_1	X_2	X_3	X_4	X_1	X_2	X_3	X_4
S_1	1	-/(1)*	0	-	0	-/(0)*	1	-
S_2	-/(1)*	1	-	0	-(0)*	0	-	1
S_1 (S_2)	1	0/(1)*	0	0	0	0/(0)*	1	0
S_2 (S_1)	0/(1)*	1	0	0	0/(0)*	0	0	1

Partial Active Redundancy (1/0)*

Passive Redundancy ($S_{1,2}$)